IN THE SPECIFICATION:

**Please amend paragraph [0003] as follows:**

[0003] The term "patterning device" as will be employed herein should be broadly interpreted to refer to ~~means~~ a device that can be used to endow an incoming radiation beam with a patterned cross-section, corresponding to a pattern that is to be created in a target portion of the substrate. The term "light valve" may also be used in this context. Generally, the pattern will correspond to a particular functional layer in a device being created in the target portion, such as an integrated circuit or other device (see below). Examples of such patterning devices include:

**Please amend paragraph [0005] as follows:**

(b) *a programmable mirror array*: an example of such a device is a matrix-addressable surface having a viscoelastic control layer and a reflective surface. The basic principle behind such an apparatus is that (for example) addressed areas of the reflective surface reflect incident light as diffracted light, whereas unaddressed areas reflect incident light as undiffracted light. Using an appropriate filter, the ~~said~~ undiffracted light can be filtered out of the reflected beam, leaving only the diffracted light behind; in this manner, the beam becomes patterned according to the addressing pattern of the matrix-addressable surface. The required matrix addressing can be performed using suitable electronic means. More information on such mirror arrays can be gleaned, for example, from United States Patent Nos. US 5,296,891 and US 5,523,193, which are incorporated herein by reference. In the case of a programmable mirror array, the ~~said~~ support structure may be embodied as a frame or table, for example, which may be fixed or movable as required; and

**Please amend paragraph [0039] as follows:**

Returning to FIG. 2A, process 200 progresses to procedure task P203 to select the photoresist to be applied to the wafer substrate W. In one embodiment, the photoresist selected enables the creation of a high contrast latent image while exhibiting reduced memory reaction characteristics. A ~~Reduced~~ reduced memory photoresist reaction process ~~characteristics refer~~ refers to a process in which the effects of an initial exposure on the photoresist are, to a certain extent, dissipated.

**Please amend paragraph [0048] as follows:**

[0048] In an alternative embodiment, indicated by the dashed lines of FIG. 2A, after procedure task P208, which directs the baking of the wafer substrate W having sub-pattern $T_1$ imaged on the photoresist, process 200 progresses to procedure block P210A, where wafer substrate W is directed a development station that applies a developing solution to substrate W to remove the ~~unexposed~~ exposed photoresist material associated with the exposure of the first sub-pattern $T_1$. Then, in procedure task P212A, the substrate W is directed back to lithographic apparatus 100, where the substrate W is shifted or offset by a predetermined distance $\Delta D$. As noted above, predetermined distance $\Delta D$ corresponds to the shift necessary to adequately image the features of the second sub-pattern $T_2$ on the photoresist in order to superimpose the second sub-pattern $T_2$ features in between the features of the already-imaged first sub-pattern $T_1$ so as to render the original desired target pattern T.

**Please amend paragraph [0050] as follows:**

[0050] The substrate W is subsequently directed, once again, to a development station and other post-exposure processes, as indicated in procedure block P218A, where a developer solution is applied to the substrate W to remove the ~~unexposed~~ exposed photoresist material associated with the exposure of the second sub-pattern $T_2$ and to prepare the substrate W for further processing.